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abacom splan 7 0This invention relates generally to semiconductor devices and more particularly to a semiconductor device having improved source/drain regions and improved junction depths which are useful in improving device performance. In semiconductor devices such as MOSFETs (Metal Oxide Semiconductor Field Effect Transistors), there is a continuous drive to downscale device dimensions. MOSFET downscaling requires ultra shallow source and drain regions to avoid punch through or excessive drain leakage and to improve performance. A source/drain region can be made ultra shallow in practice, and in conventional fabrications becomes shallower due to dopant activation anneals and high temperature stress in the source/drain regions during processing of device. For example, there is a reported need to make an ultra shallow source/drain region less than 20 nm for a typical MOSFET device. Dopant activation anneals and high temperature stresses are known to result in a significant increase in the junction depth of ultra shallow source/drain regions. As channel lengths are reduced in MOSFETs, the drive current increases but the short channel effect (SCE) also increases. The SCE, which is the statistical variation in the current due to statistical variation in the device channel length, is a problem which can be mitigated by making the transistor channel short. In a conventional MOSFET device, there is a need to have a minimum channel length for a given current target for

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